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EXAMINER	
REDDIVALAM, SRINIVASA R	
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2477	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/827,433	MIZUTANI ET AL.
	Examiner	Art Unit
	SRINIVASA R. REDDIVALAM	2477

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/09/2009 has been entered.

Claim Objections

2. Claim **8 and 13** are objected to because of the following informalities: In line 2 of each of the claims, the words 'output step are executed' need to be changed to the words 'output step **is** executed'. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-4 and 6-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horvath et al. (US Patent Number: 5,630,056) in view of Meyers et al. (Publication No: EP 0747803 A2).

Regarding claim 1, Horvath et al. teach a data processing apparatus that has a plurality of reception interface sections which receive same data from a same data sender and processes data, received by said plurality of reception interface sections, in parallel, **(**see Fig.2, interfaces 14a, 14b for plurality of reception interface sections and **see col.4, lines 17-23 wherein the interface sections 14a & 14b, each of which responding in lock step synchronism with the other to identical information input signals from the bus is mentioned** and also see col.2, lines 25-32 wherein a digital data processing device with plurality of functional units **processing data in parallel** is mentioned and col.2, lines 54-59 wherein transceivers, which include both transmitters and receivers, routing data is mentioned**),** comprising:

wherein each of said reception interface sections includes a communication error processing section **(**see col.2, lines 54-59 wherein transceivers routing data to the fault-detector is mentioned and also see Fig.2, block 40 for Error Detect/fault detector which is equivalent to communication error processing section**)** which, upon occurrence of an error in said received data by one of said reception interface sections, stops receiving said data, and requests said data sender to resend data **(**see col.2, lines 32-36 wherein

fault-detector signaling a fault is mentioned and also see col.2, lines 47-53 wherein upon detection of error, functional unit disabling the processing sections further from applying signals and responding to the error by reapplying the data is mentioned. And also see Fig.1 and col.3, line 55 to col.4, line 2 wherein functional units i.e. processor/memory elements 10, 12 partnered with one another to respond concurrently and identically to information input from bus 20 to generate further information for output to bus 20 is mentioned, likewise peripheral device controllers 14, 16 partnered with one another to process and communicate like information between the functional units and peripheral devices is mentioned).

Horvath et al. do not teach specifically the apparatus comprising a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of said reception interface sections and said data sender, wherein each of said reception interface sections receives data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal supplied from said frequency divider, from said data sender according to said sync signal, wherein upon occurrence of an error in said received data by one of said reception interface sections, sends a communication error signal to all other of said reception interface sections to stop data reception from said data sender, wherein each of said reception interface sections includes an arithmetic operation unit, an I/0 unit, and a memory bridge that provides data from said arithmetic operation unit to said I/0 unit of the respective reception interface section, wherein said error in said received data is

detected by said memory bridge of said one of said reception interface sections, and wherein said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections.

However, Meyers et al. teach an apparatus comprising a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of reception interface sections and said data sender (see Fig.1A for an apparatus and see page 49, lines 19-24 wherein deriving *both T_CLK and the local CLK/RCV_CLK sync signals with the same frequency* from the same clock signal/predetermined clock signal is mentioned and see Figure 2 for CPU of Fig.1A/apparatus, Fig.6 for X/Y interface units of CPU & Figs. 7A & 7B for generating/applying T_CLK & RCV_CLK sync signals to XMT_Register & CS_FIFO/buffer of X/Y interface units of CPU is mentioned), wherein each of said reception interface sections receives data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal supplied from said frequency divider, from said data sender according to said sync signal (see Figs. 7A & 7B and page 15, line 36 to page 16, line 3 wherein CS_FIFO 102x/y of X/Y Interface units receiving 9-bit symbols/data at RCV Register 124 being held in one T_CLK period from the transmitting entity/router is mentioned and also coupling of each symbol in the XMT_Register 120 of the router to RCV Register 124 of CS_FIFO 102x/y of X/Y Interface units with the T_CLK is mentioned and also pulling symbols from the storage

queue 126 with the synchronous RCV_CLK and operating T_CLK and RCV_CLK in frequency locked mode to avoid overflow or underflow of data in CS FIFO 102x/y of X/Y Interface units is mentioned),

wherein upon occurrence of an error in received data by one of reception interface sections, sends a communication error signal to all other of reception interface sections to stop data reception from data sender (see Figs. 1A, 2, 6 and 8 and page 14, lines 1-28 wherein upon encountering an error by one interface unit, issuing the error signal or passing of the message packet information by one interface unit to the companion interface unit for cross-checking for errors is mentioned), wherein each of said reception interface sections includes an arithmetic operation unit , an I/0 unit, and a memory bridge that provides data from said arithmetic operation unit to said I/0 unit of the respective reception interface section (see Figures 1A and 2 wherein Processor_Unit/ arithmetic_operation_unit inside the CPU 12A, blocks 14A/16A in Fig.1A for an I/O unit and block 24a/b for Interface unit/memory bridge in Fig.2 are shown **and** also see Fig.1A and page 10, lines 20-25 wherein block 24a/b i.e. Interface unit/memory bridge providing/handling all I/O traffic/data between CPU 12A and I/O unit is mentioned),

wherein said error in said received data is detected by said memory bridge of said one of said reception interface sections and wherein said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections (see Figs. 6 and 8 and page 14, lines 1-28 wherein upon encountering an error by one interface_unit/memory_bridge, issuing the error signal or passing of the message packet information by one

interface_unit/memory_bridge to the companion interface_unit/memory_bridge for cross-checking for errors is mentioned).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the apparatus of Horvath et al. to include a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of said reception interface sections and said data sender, wherein each of said reception interface sections receives data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal supplied from said frequency divider, from said data sender according to said sync signal, wherein upon occurrence of an error in received data by one of said reception interface sections, sending a communication error signal to all other of reception interface sections to stop data reception from data sender, wherein each of said reception interface sections including an arithmetic operation unit , an I/0 unit, and a memory bridge that provides data from said arithmetic operation unit to said I/0 unit of the respective reception interface section, wherein said error in said received data is detected by said memory bridge of said one of said reception interface sections and wherein said memory bridge of said one of said reception interface sections sending the communication error signal to said other memory bridges of said other reception interface sections, disclosed by Meyers et al. in order to improve the reliability, provide assurance of proper data communication and optimize the performance of the data processing apparatus.

Regarding claims 2 and 3, Horvath et al. and Meyers et al. together teach the data processing apparatus according to claim 1.

Horvath et al. further teach the data processing apparatus, wherein when an error occurs in part of received data, said communication error processing section of each of said reception interface sections cancels said error-occurred data, and requests said data sender to resend said canceled data (see col.2, lines 37-53 wherein upon detection of an error by fault-detector, disabling of data processing by functional unit and re-transmission of respective data by processing sections are mentioned) and wherein said data sender sends same serial data (see col.2, lines 54-59 wherein transceiver routing data is mentioned), and when an error occurs in received serial data, said communication error processing section of each of said reception interface sections cancels said error-occurred serial data and serial data received following that error-occurred serial data, and requests said data sender to resend said canceled serial data (see col.2, lines 47-53 and lines 58-65 wherein upon detection of an error by fault-detector, disabling of processing section from applying data and re-transmission of serial data by transceiver to fault-detector are mentioned).

Regarding claim 4, Horvath et al. and Meyers et al. together teach the data processing apparatus according to claim 1.

Horvath et al. further teach the data processing apparatus wherein data sender sends data packet when an error occurs in data of the received packet (see col.2, lines 62-65)

and said communication error processing section of each of said reception interface sections requests said data sender to resend data (see col.2, lines 32-36).

Horvath et al. do not teach yet the data processing apparatus wherein data sender affixing a sequence number to each packet when sending data packets when an error occurs in data of received packet and communication error processing section requesting data sender to resend data packets based on sequence number affixed to each received packet.

However, Meyers et al. teach the data processing apparatus wherein data sender affixing a sequence number to each packet when sending data packets when an error occurs in data of received packet and communication error processing section requesting data sender to resend data packets based on sequence number affixed to each received packet (see Fig. 35 and page 60, line 49 to page 61, line 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the apparatus of Horvath et al. to have the data sender affixing a sequence number to each packet when sending data packets when an error occurs in data of received packet and communication error processing section requesting data sender to resend data packets based on sequence number affixed to each received packet, disclosed by Meyers et al. in order to improve the reliability, provide assurance

of proper data communication and optimize the performance of the data processing apparatus.

Regarding claim 6, Horvath et al. teach a data processing apparatus that has a transmission interface section which transmits transmission data to a plurality of data receivers at a same timing (see col.2, lines 25-29 wherein a digital data processing device transmitting data between plural functional units is mentioned and also **see col.4, lines 17-23 wherein the interface sections 14a & 14b, each of which responding in lock step synchronism with the other to identical information input signals from the bus is mentioned**).

Horvath et al. do not teach specifically data processing apparatus comprising a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to said transmission interface section and said plurality of data receivers, wherein said transmission interface section generates packet data by dividing said transmission data to data of a data length shorter than one period length of said signal supplied from said frequency divider and sends individual pieces of packet data generated to said plurality of receivers at the same timing in synchronism with said clock signal.

However, Meyers et al. teach a data processing apparatus comprising a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock

signal and sends said generated sync signal to said transmission interface section and said plurality of data receivers (see Fig.1A for an apparatus and see page 49, lines 19-24 wherein deriving *both T_CLK and the local CLK/RCV_CLK sync signals with the same frequency* from the same clock signal/predetermined clock signal is mentioned and see Figure 2 for CPU of Fig.1A/apparatus, Fig.6 for X/Y interface units of CPU & Figs. 7A & 7B for generating/applying T_CLK & RCV_CLK sync signals to XMT_Register & CS_FIFO/buffer of X/Y interface units of CPU is mentioned), wherein transmission interface section generates packet data by dividing transmission data to data of a data length shorter than one period length of sync signal supplied from said frequency divider and sends individual pieces of packet data generated to plurality of receivers at the same timing in synchronism with said clock signal (see Figs. 7A & 7B and page 15, line 36 to page 16, line 3 wherein CS_FIFO 102x/y of X/Y Interface units receiving 9-bit symbols/data at RCV Register 124 being held in one T_CLK period from the transmitting entity/router is mentioned and also coupling of each symbol in the XMT_Register 120 of the router to RCV Register 124 of CS_FIFO 102x/y of X/Y Interface units with the T_CLK is mentioned and also pulling symbols from the storage queue 126 with the synchronous RCV_CLK and operating T_CLK and RCV_CLK in frequency locked mode to avoid overflow or underflow of data in CS FIFO 102x/y of X/Y Interface units is mentioned and also see page 16, lines 47-59 & pages 47-48, section synchronization).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the data processing apparatus of Horvath et al. to have a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to said transmission interface section and said plurality of data receivers and to include transmission interface section generating packet data by dividing transmission data to data of a data length shorter than one period length of sync signal supplied from frequency divider and sending individual pieces of packet data generated to plurality of receivers at the same timing in synchronism with said clock signal disclosed by Meyers et al. to provide both assurance of proper data communication and data synchronization between transmission and reception sections of data processing in the system.

Regarding claim 7, Horvath et al. teach a data processing method that performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender (see col.2, lines 25-32 wherein a digital data processing device with plurality of functional units processing data in parallel is mentioned and col.2, lines 54-59 wherein transceivers routing data is mentioned and also **see col.4, lines 17-23 wherein the interface sections 14a & 14b, each of which responding in lock step synchronism with the other to identical information input signals from the bus is mentioned)** and comprises: a data reception step of receiving data from said data sender at each of said plurality of reception interface sections (see col.2, lines 54-59 wherein transceivers sending data to fault-detector is mentioned);
an error detection step of detecting an error in said received data by one of said

reception interface sections (see col.2, lines 32-36 wherein fault-detector signaling a fault of received data is mentioned);

Horvath et al. do not teach specifically the method comprises *a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender; a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal*; an error information output step of outputting information on said detected error by said one of said reception interface sections to all other of said reception interface sections, wherein each of said reception interface sections includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of said respective reception interface section, wherein said error detection step comprises detecting said error in said received data by said memory bridge of said one of said reception interface sections, and wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections.

However, Meyers et al. teach the method comprising *a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender* (see Fig.1A for an apparatus and see page 49, lines 19-24 wherein deriving *both T_CLK and the local CLK/RCV_CLK sync signals with the same frequency* from the same clock signal/predetermined clock signal is mentioned and see Figure 2 for CPU of Fig.1A/apparatus, Fig.6 for X/Y interface units of CPU & Figs. 7A & 7B for generating/applying T_CLK & RCV_CLK sync signals to XMT_Register & CS_FIFO/buffer of X/Y interface units of CPU is mentioned); *a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal* (see Figs. 7A & 7B and page 15, line 36 to page 16, line 3 wherein CS_FIFO 102x/y of X/Y Interface units receiving 9-bit symbols/data at RCV Register 124 being held in one T_CLK period from the transmitting entity/router is mentioned and also coupling of each symbol in the XMT_Register 120 of the router to RCV Register 124 of CS_FIFO 102x/y of X/Y Interface units with the T_CLK is mentioned and also pulling symbols from the storage queue 126 with the synchronous RCV_CLK and operating T_CLK and RCV_CLK in frequency locked mode to avoid overflow or underflow of data in CS FIFO 102x/y of X/Y Interface units is mentioned); an error information output step of outputting information on detected error by one of reception interface sections to all other reception interface sections (see Figs. 1A, 2, 6 and 8 and

page 14, lines 1-28 wherein upon encountering an error by one interface unit, issuing the error signal or passing of the message packet information by one interface unit to the companion interface unit for cross-checking for errors is mentioned), wherein each of said reception interface sections includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of said respective reception interface section (see Figures 1A and 2 wherein Processor_Unit/ arithmetic_operation_unit inside the CPU 12A, blocks 14A/16A in Fig.1A for an I/O unit and block 24a/b for Interface unit/memory bridge in Fig.2 are shown **and** also see Fig.1A and page 10, lines 20-25 wherein block 24a/b i.e. Interface unit/memory bridge providing/handling all I/O traffic/data between CPU 12A and I/O unit is mentioned), wherein said error detection step comprises detecting said error in said received data by said memory bridge of said one of said reception interface sections and wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections (see Figs. 6 and 8 and page 14, lines 1-28 wherein upon encountering an error by one interface_unit/memory_bridge, issuing the error signal or passing of the message packet information by one interface_unit/memory_bridge to the companion interface_unit/memory_bridge for cross-checking for errors is mentioned).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the method of Horvath et al. to include steps of *a frequency division*

step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender; a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal; an error information output step of outputting information on detected error by said one of said reception interface sections to all other of said reception interface sections, wherein each of said reception interface sections including an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of said respective reception interface section, wherein said error detection step comprising detecting said error in said received data by said memory bridge of said one of said reception interface sections and wherein said error information output step comprising sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections, disclosed by Meyers et al. in order to improve the reliability, provide assurance of proper data communication and optimize the performance of the data processing of apparatus.

Regarding claim 8, Horvath et al. and Meyers et al. together teach the data processing method according to claim 7.

Horvath et al. do not teach specifically the method wherein said error information output step is executed according to said sync signal.

However, Meyers et al. teach the data processing method wherein said error information output step is executed according to a sync signal (see page 14, lines 32-42 and also see page 16, lines 47-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the method of Horvath et al. to have information output step executed according to a sync signal, disclosed by Meyers et al. in order to improve the reliability, provide assurance of proper data communication and optimize the performance of the data processing apparatus.

Regarding claim 9, Horvath et al. further teach the data processing method comprising a data resend requesting step of requesting said data sender to resend data in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step (see col.2, lines 32-53 wherein fault-detector signaling a fault is mentioned and wherein upon detection of an error by fault-detector, disabling of data processing by functional unit and re-transmission of respective data by processing sections are mentioned).

Horvath et al. do not teach specifically the method comprising an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections.

However, Meyers et al. teach the data processing method comprising an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections (see Figs. 6

and 8 and page 14, lines 1-28 wherein upon encountering an error by one interface unit, issuing the error signal or passing of the message packet information by one interface unit to the companion interface unit for cross-checking for errors is mentioned).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the method of Horvath et al. to include an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections, disclosed by Meyers et al. in order to improve the reliability, provide assurance of proper data communication and optimize the performance of the data processing apparatus.

Regarding claim 10, Horvath et al. and Meyers et al. together teach the data processing method according to claim 9.

Horvath et al. further teach the data processing method further comprising a data cancellation step of canceling data and a data reception stopping step of stopping data reception and wherein said data cancellation step and said data reception stopping step are executed in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step (see col.2, lines 47-53 wherein upon detection of error, functional unit disabling the processing sections further from applying signals is mentioned), and said data resend requesting step requests resending of data canceled at said data cancellation step (see col.2, lines 58-65 wherein upon detection of an error by fault-detector, re-transmission of serial data by transceiver to fault-detector is mentioned).

Regarding claim 11, Horvath et al. and Meyers et al. together teach the data processing method according to claim 10.

Horvath et al. do not teach specifically the method wherein said data cancellation step is executed according to said sync signal.

However, Meyers et al. teach the data processing method wherein said data cancellation step is executed according to said sync signal (see page 15, lines 2-8, and also page 16, lines 47-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the method of Horvath et al. to have data cancellation step executed according to said sync signal, disclosed by Meyers et al. in order to improve the reliability, provide assurance of proper data communication and optimize the performance of the data processing apparatus.

Regarding claim 12, Horvath et al. teach a computer readable medium having thereon a computer program, which when executed, (see col.4, lines 60-62 wherein a device implementation in software/hardware is mentioned) performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender (see col.2, lines 25-32 wherein a digital data processing device with plurality of functional units processing data in parallel is mentioned and col.2, lines 54-59 wherein transceivers routing data is mentioned and also **see col.4, lines 17-23 wherein the interface sections 14a & 14b, each of which responding in lock step synchronism with the other to identical information input signals from**

the bus is mentioned) and allows a computer to execute: a data reception step of receiving data from said data sender at each of said plurality of reception interface sections (see col.2, lines 54-59 wherein transceivers sending data to fault-detector is mentioned);

an error detection step of detecting an error in said received data by one of said reception interface sections (see col.2, lines 32-36 wherein fault-detector signaling a fault of received data is mentioned);

Horvath et al. do not teach the above medium that allows a computer to execute *a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender; a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal*; an error information output step of outputting information on said detected error by said one of said reception interface sections to all other of said reception interface sections, wherein each of said reception interface sections includes an arithmetic operation unit, an I/0 unit, and a memory bridge that provides data from said arithmetic operation unit to said I/0 unit of said respective reception interface section, wherein said error detection step comprises detecting said error in said received data by said memory bridge of said one of said reception interface sections, and

wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections.

However, Meyers et al. teach the computer readable medium that allows a computer to execute *a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender* (see Fig.1A for an apparatus and see page 49, lines 19-24 wherein deriving *both T_CLK and the local CLK/RCV_CLK sync signals with the same frequency* from the same clock signal/predetermined clock signal is mentioned and see Figure 2 for CPU of Fig.1A/apparatus, Fig.6 for X/Y interface units of CPU & Figs. 7A & 7B for generating/applying T_CLK & RCV_CLK sync signals to XMT_Register & CS_FIFO/buffer of X/Y interface units of CPU is mentioned)*; a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal* (see Figs. 7A & 7B and page 15, line 36 to page 16, line 3 wherein CS_FIFO 102x/y of X/Y Interface units receiving 9-bit symbols/data at RCV Register 124 being held in one T_CLK period from the transmitting entity/router is mentioned and also coupling of each symbol in the XMT_Register 120 of the router to RCV Register 124 of CS_FIFO 102x/y of X/Y Interface units with the T_CLK is

mentioned and also pulling symbols from the storage queue 126 with the synchronous RCV_CLK and operating T_CLK and RCV_CLK in frequency locked mode to avoid overflow or underflow of data in CS FIFO 102x/y of X/Y Interface units is mentioned); an error information output step of outputting information on detected error by one of reception interface sections to all other of said reception interface sections (see Figs. 1A, 2, 6 and 8 and page 14, lines 1-28 wherein upon encountering an error by one interface unit, issuing the error signal or passing of the message packet information by one interface unit to the companion interface unit for cross-checking for errors is mentioned), wherein each of said reception interface sections includes an arithmetic operation unit, an I/0 unit, and a memory bridge that provides data from said arithmetic operation unit to said I/0 unit of said respective reception interface section (see Figures 1A and 2 wherein Processor_Unit/ arithmetic_operation_unit inside the CPU 12A, blocks 14A/16A in Fig.1A for an I/O unit and block 24a/b for Interface unit/memory bridge in Fig.2 are shown **and** also see Fig.1A and page 10, lines 20-25 wherein block 24a/b i.e. Interface unit/memory bridge providing/handling all I/O traffic/data between CPU 12A and I/O unit is mentioned), wherein said error detection step comprises detecting said error in said received data by said memory bridge of said one of said reception interface sections and wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections (see Figs. 6 and 8 and page 14, lines 1-28 wherein upon encountering an error by one interface_unit/memory_bridge, issuing the error signal or

passing of the message packet information by one interface_unit/memory_bridge to the companion interface_unit/memory_bridge for cross-checking for errors is mentioned).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the computer readable medium of Horvath et al. to allow a computer to execute *a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender; a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal*, and an error information output step of outputting information on detected error by said one of said reception interface sections to all other of said reception interface sections, wherein each of said reception interface sections including an arithmetic operation unit, an I/0 unit, and a memory bridge that provides data from said arithmetic operation unit to said I/0 unit of said respective reception interface section, wherein said error detection step comprising detecting said error in said received data by said memory bridge of said one of said reception interface sections and wherein said error information output step comprising sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other

memory bridges of said other reception interface sections, disclosed by Meyers et al. in order to improve the reliability, provide assurance of proper data communication and optimize the performance of the data processing of apparatus.

Regarding claim 13, Horvath et al. and Meyers et al. together teach the computer readable medium according to claim 12.

Horvath et al. do not teach specifically the medium wherein said error information output step is executed according to said sync signal.

However, Meyers et al. teach the medium wherein said error information output step is executed according to a sync signal (see page 14, lines 32-42 and also see page 16, lines 47-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the medium of Horvath et al. to have information output step executed according to a sync signal, disclosed by Meyers et al. in order to improve the reliability, provide assurance of proper data communication and optimize the performance of the data processing apparatus.

Regarding claim 14, Horvath et al. further teach the medium wherein said computer is allowed to further execute: a data resend requesting step of requesting said data sender to resend data in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step (see col.2, lines 32-53 wherein fault-detector signaling a fault is mentioned and wherein upon detection of an error by fault-detector, disabling of data

processing by functional unit and re-transmission of respective data by processing sections are mentioned).

Horvath et al. do not teach specifically the medium wherein said computer is allowed to further execute an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections.

However, Meyers et al. teach the medium wherein said computer is allowed to further execute an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections (see Figs. 6 and 8 and page 14, lines 1-28 wherein upon encountering an error by one interface unit, issuing the error signal or passing of the message packet information by one interface unit to the companion interface unit for cross-checking for errors is mentioned).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the medium of Horvath et al. to include an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections, disclosed by Meyers et al. in order to improve the reliability, provide assurance of proper data communication and optimize the performance of the data processing apparatus.

Regarding claim 15, Horvath et al. and Meyers et al. together teach the computer readable medium according to claim 14.

Horvath et al. further teach the computer readable medium according to claim 14, executing a data cancellation step of canceling data; and a data reception stopping step of stopping data reception, and wherein said data cancellation step and said data reception stopping step are executed in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step (see col.2, lines 47-53 wherein upon detection of error, functional unit disabling the processing sections further from applying signals is mentioned), and said data resend requesting step requests resending of data canceled at said data cancellation step (see col.2, lines 58-65 wherein upon detection of an error by fault-detector, re-transmission of serial data by transceiver to fault-detector is mentioned).

Regarding claim 16, Horvath et al. and Meyers et al. together teach the computer readable medium according to claim 15.

Horvath et al. do not teach specifically the medium wherein said data cancellation step is executed according to said sync signal.

However, Meyers et al. teach the medium wherein said data cancellation step is executed according to said sync signal (see page 15, lines 2-8, and also page 16, lines 47-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the medium of Horvath et al. to have data cancellation step executed according to said sync signal, disclosed by Meyers et al. in order to improve

the reliability, provide assurance of proper data communication and optimize the performance of the data processing apparatus.

Regarding claims 17-19, Horvath et al. and Meyers et al. together teach the data processing apparatus/data processing method/the computer readable medium according to claims 1, 7 and 12 respectively.

Horvath et al. **do not teach** specifically the data processing apparatus wherein said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections as an open drain signal and **do not teach** specifically the data processing method/the computer readable medium wherein in said error information output step, said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections as an open drain signal.

However, Meyers et al. teach the data processing apparatus wherein said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections as an open drain signal (see Figures 5 and 10 and page 19, lines 34-54 wherein each memory interface 70a/b of Interface_unit/memory_bridge receiving and comparing data bits and asserting/sending an error_signal/ECC_logic_error_signal/open_drain_signal on detecting error condition is

mentioned) and teach the data processing method/the computer readable medium wherein in said error information output step, said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections as an open drain signal (see Figures 5 and 10 and page 19, lines 34-54 wherein each memory interface 70a/b of Interface_unit/memory_bridge receiving and comparing data bits and asserting/sending an error_signal/ECC_logic_error_signal/open_drain_signal on detecting error condition is mentioned).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the data processing apparatus/data processing method/the computer readable medium of Horvath et al. to have memory bridge of said one of said reception interface sections sending the communication error signal to said other memory bridges of said other reception interface sections as an open drain signal in said error information output step, disclosed by Meyers et al. in order to improve the reliability and provide both assurance of proper data communication and data integrity in the system.

Regarding claim 20, Horvath et al. and Meyers et al. together teach the data processing apparatus according to claim 1.

Horvath et al. do not teach specifically the apparatus wherein a difference occurs in a timing that the plurality of reception interface sections receives

the same data, and wherein the plurality of reception interface sections receive the same data within a same period of said sync signal.

However, Meyers et al. teach an apparatus wherein a difference occurs in a timing that the plurality of reception interface sections receives the same data, and wherein the plurality of reception interface sections receive the same data within a same period of said sync signal (*see Figs. 7A & 7B and page 15, line 16 to page 16, line 50 wherein the function of CS_FIFO 102x/y of X/Y Interface units to accommodate the possible difference between the clock of router 14 used to transmit symbols to CPU 12 and the clock used by interface unit 24 to receive those symbols is mentioned and wherein CS_FIFO 102x/y of X/Y Interface units receiving 9-bit symbols/data at RCV Register 124 being held in one T_CLK period from the transmitting entity/router is mentioned and also coupling of each symbol in the XMT_Register 120 of the router to RCV Register 124 of CS_FIFO 102x/y of X/Y Interface units with the T_CLK is mentioned*).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the apparatus of Horvath et al. to have difference occurring in a timing that the plurality of reception interface sections receives the same data, and wherein the plurality of reception interface sections receive the same data within a same period of said sync signal, disclosed by Meyers et al. to provide both assurance of proper data communication and data synchronization between transmission and reception sections of data processing in the system.

Regarding claim 21, Horvath et al. and Meyers et al. together teach the data processing method according to claim 7.

Horvath et al. do not teach specifically the method comprising receiving the same data at different points in time by the plurality of reception interface sections, wherein the plurality of reception interface sections receive the same data within a same period of said sync signal.

However, Meyers et al. teach the method comprising receiving the same data at different points in time by the plurality of reception interface sections, wherein the plurality of reception interface sections receive the same data within a same period of said sync signal (*see Figs. 7A & 7B and page 15, line 16 to page 16, line 50 wherein the function of CS_FIFO 102x/y of X/Y Interface units to accommodate the possible difference between the clock of router 14 used to transmit symbols to CPU 12 and the clock used by interface unit 24 to receive those symbols is mentioned and wherein CS_FIFO 102x/y of X/Y Interface units receiving 9-bit symbols/data at RCV Register 124 being held in one T_CLK period from the transmitting entity/router is mentioned and also coupling of each symbol in the XMT_Register 120 of the router to RCV Register 124 of CS_FIFO 102x/y of X/Y Interface units with the T_CLK is mentioned*).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the method of Horvath et al. to include receiving the same data at different points in time by the plurality of reception interface sections, wherein the plurality of reception interface sections receive the same data within a same period

of said sync signal, disclosed by Meyers et al. to provide both assurance of proper data communication and data synchronization between transmission and reception sections of data processing in the system.

Response to Arguments

6. Applicant's arguments filed on 10/09/2009 with respect to claims 1-4 and 6-21 have been considered but they are not persuasive. Applicant's amendment of independent claims 1, 6, 7 & 12 and added new claims 20-21 necessitated new citations of references as presented in this office action.

7. In page 10 of Remarks, regarding amended independent claims 1, 6, 7 & 12, Applicants mainly mention that neither Horvath et al. nor Meyers et al. teach or suggest *a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of said reception interface sections and said data sender, in which each of said reception interface sections receives data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal supplied from said frequency divider, from said data sender according to said sync signal.*

However, the **Examiner respectfully disagrees to the above statements of the Applicant** as Meyers et al. teach an apparatus comprising a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of reception interface sections and said

data sender (see Fig.1A for an apparatus and see page 49, lines 19-24 wherein deriving *both T_CLK and the local CLK/RCV_CLK sync signals with the same frequency* from the same clock signal/predetermined clock signal is mentioned and see Figure 2 for CPU of Fig.1A/apparatus, Fig.6 for X/Y interface units of CPU & Figs. 7A & 7B for generating/applying T_CLK & RCV_CLK sync signals to XMT_Register & CS_FIFO/buffer of X/Y interface units of CPU is mentioned), in which each of said reception interface sections receives data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal supplied from said frequency divider, from said data sender according to said sync signal (see Figs. 7A & 7B and page 15, line 36 to page 16, line 3 wherein CS_FIFO 102x/y of X/Y Interface units receiving 9-bit symbols/data at RCV Register 124 being held in one T_CLK period from the transmitting entity/router is mentioned and also coupling of each symbol in the XMT_Register 120 of the router to RCV Register 124 of CS_FIFO 102x/y of X/Y Interface units with the T_CLK is mentioned and also pulling symbols from the storage queue 126 with the synchronous RCV_CLK & operating T_CLK and RCV_CLK in frequency locked mode to avoid overflow or underflow of data in CS FIFO 102x/y of X/Y Interface units is mentioned which is equivalent to each of said reception interface sections receives data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal supplied from said frequency divider, from said data sender according to said sync signal) and thus Horvath et al. in combination with Meyers et al. teach all the limitations of claims 1, 6, 7 & 12 as already mentioned above under Claim Rejections.

8. The rejection of all other dependent claims is already explained above under Claim Rejections.

Conclusion

9. Any response to this office action should be faxed to (571) 273-8300 or mailed

To:

Commissioner for Patents,
P.O. Box 1450
Alexandria, VA 22313-1450
Hand-delivered responses should be brought to
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SRINIVASA R. REDDIVALAM whose telephone number is (571)270-3524. The examiner can normally be reached on Mon-Fri 9:30 AM - 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag Shah can be reached on 571-272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Srini Reddivalam
12/14/2009

/Gregory B Sefcheck/
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12-14-2009